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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,975	05/16/2005	Nicolas Pangaud	ASK-004	1734

32954 7590 04/18/2007

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EXAMINER	
CHOE, YONG J	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,975	PANGAUD, NICOLAS	
	Examiner	Art Unit	
	Yong Choe	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/16/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/534975 has a total of 8 claims pending in the application. Claims 1-10 have been canceled. There are 2 independent claims (e.g., claim 11 and 17) and 6 dependent claims, all of which are ready for examination by the examiner.

Priority

2. As required by M.P.E.P. 201.14(c), acknowledgment is made of applicant's claim for priority based on an application filed on 12/12/2003.

Information Disclosure Statement

3. As required by M.P.E.P. 609 (C), the applicant's submission of the information Disclosure Statement dated 05/16/2005 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

Oath/Declaration

4. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Drawings

5. The drawings submitted on 05/16/2005 are acceptable for examination purposes.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 11-18** are rejected under 35 U.S.C. 102(e) as being anticipated by **Kusakabe et al. (US Patent No.: US 6,330,633).**

Regarding independent claims 11 and 17, Kusakabe discloses a method for modifying the data in a card transaction system including a smart card (Fig.1: IC CARD 2) or the like and a reader (Fig.1: READER) capable of reading said card (Fig.1: IC CARD 2) when it is in a determined position in relation to said reader (Fig.1: READER), said card (Fig.1: IC CARD 2) including a non-volatile, erasable and rewritable memory comprising at least one location to record a data value relating to the transactions carried out by said card (Fig.1: IC CARD 2), each transaction causing the incrementation of said data value (col.1, lines 16-21: The IC card incorporates a CPU (Central Processing Unit) for carrying out various kinds of processing and a memory for storing data or the like necessary for processing in which transmitting and receiving of

data is carried out in a state where the IC card is brought into contact with a predetermined reader/writer);

said method comprising, at each transaction, an operation for writing said data value performs the writing of the new data value (Y) in a first location (B) (Fig.4A: 2nd REGION) which contains the value zero among two predefined locations (Fig.4A: 1st and 2nd REGIONS) forming a counter in said memory, said writing operation performing the erasing of the old data value (X) recorded in the second location (A) (Fig.4C: 1st REGION) of said two locations (see Fig.4A-C) such that, at the end of the writing operation, said first location (Fig.4C: 2nd REGION) contains said new data value (Fig.4C: new data 02,11,12,13,14,15,16,17,18,P1 and P2) whilst said second location (Fig.4C: 1st REGION) contains the value zero if this writing operation was performed correctly (Fig.4A-C and; col.1, lines 49-50 and; col.8, lines 44-49 and; col.8, lines 57-60 and; col.9, lines 4-6: The memory is provided with two blocks which are a first and second region. Fig.4A shows a situation where data 01H through 08H have already been stored in the block of the first region and data have been erased in the block of the second region. The new data is written to the block in which data has not been recorded as shown in, for example, Fig.4B. After all writing to the block which is the second region is complete, all data recorded in the block which is the first region is erased as shown in, for example, Fig.4C. Some countermeasure is needed against this memory corruption.), or

none of the two locations in said counter contains the value zero if said writing operation has not been performed correctly as a result of an abrupt withdrawal of said

card in the course of the transaction (col.9, lines 60-68: If for example the power supply fails before erasing or while erasing the old data in the step S14 or S17, it may occur that the old data remains without being erased, or only part of the data is updated so that the parity happens to be correct as shown in FIG. 5A, and memory corruption occurs. In this case, data in both of the blocks is determined to be effective in the step S11, so the routine proceeds to a step S18).

Regarding claim 12, Kusakabe teaches a repair of said counter by a rewriting operation comprising rewriting said new value (Y) in said first location (B) and erasing said old value (X) from said second location (A) when the abrupt withdrawal has taken place during the writing phase of said new value (see Fig.5A-E and col.9, lines 60-68: If for example the power supply fails before erasing or while erasing the old data in the step S14 or S17, it may occur that the old data remains without being erased, or only part of the data is updated so that the parity happens to be correct as shown in FIG. 5A, and memory corruption occurs. In this case, data in both of the blocks is determined to be effective in the step S11, so the routine proceeds to a step S18241.).

Regarding claim 13, Kusakabe teaches when said first location (B) contains an incorrect value (Y') between said old data value (X) and said new data value (Y), a repair of said counter by a rewriting operation comprising rewriting said incorrect value in said first location and erasing said old value from said second location, followed by a writing operation comprising writing said new value in said second location (A) and erasing said incorrect value from said first location (see Fig.5A-E and col.9, lines 60-

68: If for example the power supply fails before erasing or while erasing the old data in the step S14 or S17, it may occur that the old data remains without being erased, or only part of the data is updated so that the parity happens to be correct as shown in FIG. 5A, and memory corruption occurs. In this case, data in both of the blocks is determined to be effective in the step S11, so the routine proceeds to a step S18).

Regarding claim 14, Kusakabe teaches when said first location (B) contains an incorrect data value (Y') which is less than said old value (X), a repair of said counter by a rewriting operation comprising rewriting said old data value (X) in said second location (A) and erasing said incorrect data value, followed by a writing operation, comprising writing said new data value (y) in said first location and erasing said old data value from said second location (see Fig.5A-E and col.9, lines 60-68: If for example the power supply fails before erasing or while erasing the old data in the step S14 or S17, it may occur that the old data remains without being erased, or only part of the data is updated so that the parity happens to be correct as shown in FIG. 5A, and memory corruption occurs. In this case, data in both of the blocks is determined to be effective in the step S11, so the routine proceeds to a step S18).

Regarding claim 15, Kusakabe teaches a repair of said counter by a rewriting operation comprising rewriting said new data value (Y) in said first location (B) and erasing said old data value (X) from said second location (A) when the abrupt withdrawal has taken place between the writing phase of said new data value and the erasing phase of said old data value (see Fig.5A-E and col.9, lines 60-68: If for example the power supply fails before erasing or while erasing the old data in the step

S14 or S17, it may occur that the old data remains without being erased, or only part of the data is updated so that the parity happens to be correct as shown in FIG. 5A, and memory corruption occurs. In this case, data in both of the blocks is determined to be effective in the step S11, so the routine proceeds to a step S18).

Regarding claim 16, Kusakabe teaches when the abrupt withdrawal has taken place during the erasing phase of said old data value (X) and an incorrect data value (X') is recorded in said second location (A), a repair of said counter by a rewriting operation comprising rewriting said new data value (Y) in said first location (B) and erasing said incorrect data value from said second location (see Fig.5A-E and col.9, lines 60-68: If for example the power supply fails before erasing or while erasing the old data in the step S14 or S17, it may occur that the old data remains without being erased, or only part of the data is updated so that the parity happens to be correct as shown in FIG. 5A, and memory corruption occurs. In this case, data in both of the blocks is determined to be effective in the step S11, so the routine proceeds to a step S18).

Regarding claim 18, Kusakabe teaches said smart card is a contactless card (col.1, lines 31-32: data is transmitted and received between an IC card and a Reader without physical contact).

Conclusion

8. Claims rejected in the application

Per the instant office action, claims 11-18 have received a first action on the

merits and are subject of a first action non-final.

9. Any inquiry concerning this comm1unication should be directed to **Yong Choe** at telephone number **571-270-1053** or email to **yong.choe@uspto.gov**. The examiner can normally be reached on M-F 9:30am to 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Sanjiv Shah** can be reached on **571-272-4098**. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PMR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-irect.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YC
Yong J. Choe
Examiner / Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100